REMARKS

This Amendment responds to the Office Action dated March 27, 2003 in which the Examiner rejected claims 15 and 17-20 under 35 U.S.C. §103, rejected claim 16 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form and stated that claims 2-14 are allowed.

As indicated above, minor typographical errors in the specification have been corrected. It is respectfully requested that the Examiner approves the corrections.

Claim 15 claims a circuit modification method of modifying a circuit by inserting one or more buffers into a predetermined wire located within the circuit. The method comprises the steps of: first, determining whether a glitch error is caused in the predetermined wire by an aggressor comprised of one or more other wires. When a glitch error is caused in the predetermined wire by an aggressor, a number of buffers to be inserted into the predetermined wire is determined based on an amount of glitch to be caused in the predetermined wire by the aggressor.

Through the method of the claimed invention determining a number of buffers to be inserted based upon an amount of glitch, as claimed in claim 15, the claimed invention provides a circuit modification method capable of eliminating glitch errors. The prior art does not show, teach or suggest determining a number of buffers to be inserted as claimed in claim 15.

Claim 20 claims a circuit modification method comprising the steps of: first, determining whether a glitch error is caused in a predetermined wire by an aggressor comprised of one or more other wires. When a glitch error is caused in the predetermined

wire by an aggressor, a driving circuit for driving the predetermined wire is replaced with another one having a higher driving ability then the driving circuit.

Through the method of the claimed invention replacing a driving circuit with another one having a higher driving ability, as claimed in claim 20, the claimed invention provides a circuit modification method which decreases the amount of glitch. The prior art does not show, teach or suggest replacing a driving circuit as claimed in claim 20.

Claims 15 and 17-20 were rejected under 35 U.S.C. §103 as being unpatentable over *Young et al.* (U.S. Patent No. 6,378,109).

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to the claims and allows the claims to issue.

Young et al. appears to disclose methods for designing and fabricating digital integrated circuits, and in particular to simulation and analysis of the circuit design in order to detect and eliminate excessive electric field stress on gate oxide of the transistors comprising the digital circuits. (Col. 1, lines 16-20) A method is provided for designing an integrated circuit which contains a plurality of signal lines in close proximity, such that capacitive coupling among the signal lines is operable to induce crosstalk on at least one of the signal lines. Parasitics are extracted from a trial layout of the integrated circuit, and the method further comprises the steps of: grouping the plurality of signal lines into a plurality of aggressor groups; pruning the plurality of signal lines to form a plurality of victim signal lines; building a minimum region network for each victim signal line of the plurality of

victim signal lines comprising the respective victim signal line, aggressor signal lines associated with the respective victim signal line, and associated parasitics; simulating the operation of each minimum region network to determine an amount of noise induced on each respective victim signal line by the aggressor signal lines associated with the respective victim signal line, and analyzing the simulation results of each minimum region network to determine if a gate oxide integrity (GOI) violation exists. (Col. 2, line 63 through Col. 3, line 14) Selection of potential victims and their associated aggressors is a crucial step in the crosstalk verification methodology which is performed in FindVictims filtering step 711. Pruning efficiency is extremely important to reduce the crosstalk noise computation time, while not missing victims. A concept of grouping is used to perform victim/aggressor selection. A group is defined as a set of signals that could switch at the same time and hence collectively induce a glitch on a victim that is larger than if the aggressors switched at dispersed times. (Col. 9, lines 10-20) Networks having crosstalk noise violations are tabulated in step 750. In response to a detected crosstalk noise violation, the design of the IC can be modified to eliminate the violation by changing wire spacing or by insertion of repeaters in the victim signal, for example. (Col. 11, lines 57-61)

Thus, *Young et al.* merely discloses modifying the design of a IC to eliminate crosstalk noise violations by changing wire spacing or by insertion of repeaters in the victim signal. Thus nothing in *Young et al.* shows, teaches or suggests how to determine the number of buffers to be inserted as claimed in claim 15. Rather, *Young et al.* merely discloses inserting repeaters to modify the design of a IC to eliminate crosstalk noise violations. In other words, although the insertion of repeaters is stated in *Young et al.*,

Young et al. does not show, teach or suggest how to determine the number to be inserted. Thus *Young et al.* does not show, teach or suggest determining the number of buffers to be inserted based upon an amount of glitch as claimed in claim 15 nor would it be obvious to determine the number of buffers to be inserted.

Additionally, *Young et al.* merely discloses inserting repeaters to modify the design of a IC to eliminate crosstalk noise violations. Nothing in *Young et al.* shows, teaches or suggests replacing a driving circuit with another one having a higher driving ability as claimed in claim 20. Rather, *Young et al.* merely discloses insertion of (i.e. adding additional) repeaters in the victim signal to eliminate crosstalk noise violations. In other words, it would not be obvious to replace a circuit within a circuit having a different drivability when *Young et al.* merely teaches insertion of additional elements.

Since nothing in *Young et al.* shows, teaches or suggests a) determining the number of buffers to be inserted as claimed in claim 15 or b) replacing a driving circuit with another one having a higher driving ability as claimed in claim 20, it is respectfully requested that the Examiner withdraws the rejection to claims 15 and 20 under 35 U.S.C. §103.

Claims 17-19 depend from claim 15 and recite additional features. It is respectfully submitted that claims 17-19 would not have been unpatentable over *Young et al.* within the meaning of 35 U.S.C. §103 at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 17-19 under 35 U.S.C. §103.

Since objected to claim 16 depends from an allowable claim, it is respectfully requested that the Examiner withdraws the objection thereto.

New claim 21 has been added and recites additional features. It is respectfully submitted that this claim is also in condition for allowance.

Thus it now appears that the Application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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Date: June 17, 2003

Attachment to Amendment dated June 17, 2003

Mark-up of Specification

Please amend the specification as follows:

Please replace the paragraph beginning at page 6, line 13, with the following:

In accordance with a further aspect of the present invention, the wire segment number determining step is the step of, when the coupling capacity between the aggressor and the predetermined wire is Cc, the amount of the glitch is V and a predetermined value is Vmax, determining the smallest integer number n which satisfies a following relationship: [V/n Vmax] $V/n \leq Vmax$ as the number of the plurality of wire segments, and wherein the target coupling capacity calculating step is the step of calculating the target coupling capacity as follows: Cc/n, and the internal division point determining step is the step of determining the one or more internal points of division so that the coupling capacity between each of the plurality of wire segment and the aggressor is equal to the target coupling capacity Cc/n.

Please replace the paragraph beginning at page 10, line 14, with the following:

In accordance with another aspect of the present invention, the buffer number determining step is the step of, when the amount of glitch is V and a predetermined value is Vmax, calculating the smallest integer number n which satisfies a following relationship: [V/n Vmax] $V/n \leq Vmax$. By setting Vmax to a target for the amount of glitch (if the amount of glitch to be caused is equal to or less than the target, it can be assumed that the

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glitch error is eliminated), the number of buffers to be inserted is (n-1). Thus, a smaller number of buffers to be inserted can be estimated.

Replace the paragraph beginning at page 14, line 7, with the following:

A description will be made as to how the circuit is modified using the circuit modification method of the present embodiment when it is determined that a glitch caused in the wire 1 ([refereed] referred to as victim 1 hereafter) by signal change in the other wire 2 (referred to as aggressor 2 hereafter) which is an aggressor causes a glitch error, with reference to a flow chart of Fig. 5(a).

Please replace the paragraph beginning at page 15, line 13, with the following:

Next, it is determined, in step ST2, whether the amount V of glitch is equal to or less than a given value Verr or not. The value Verr is predetermined in such a manner that if the amount of glitch is greater than the value Verr, it can be determined that a glitch error occurs. If [V Verr] $V \leq Verr$, it is determined that the aggressor 2 does not cause any glitch error in the victim 1, and no circuit modification process such as insertion of one or more buffers into the victim is carried out. If $V > Verr$, it is determined that there causes a glitch error, and step ST3 is performed.

Please replace the paragraph beginning at page 16, line 18, with the following:

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In step ST31, a certain amount Vmax of glitch is predetermined, and the smallest possible integer n which satisfies the following relationship: [V/n Vmax] $V/n \leq Vmax$ is calculated. The integer n is the number by which the victim 1 is to be divided into wire segments, and the integer (n-1) is therefore equal to the number of buffers to be inserted into the victim 1. The value Vmax is a target amount of glitch which is defined as a target for the amount of glitch. If the amount of glitch to be caused is equal to or less than Vmax, it can be assumed that the glitch error is eliminated. The value Vmax is predetermined so that it simply satisfies the following relationship [Vmax Verr] $Vmax \leq Verr$. Since the relationship of [Vmax Verr V] $Vmax \leq Verr < V$ is established, the number n by which the victim 1 is to be divided is calculated and is an integer of 2 or more, and the number of buffers to be inserted into the victim is calculated and is 1 or more.